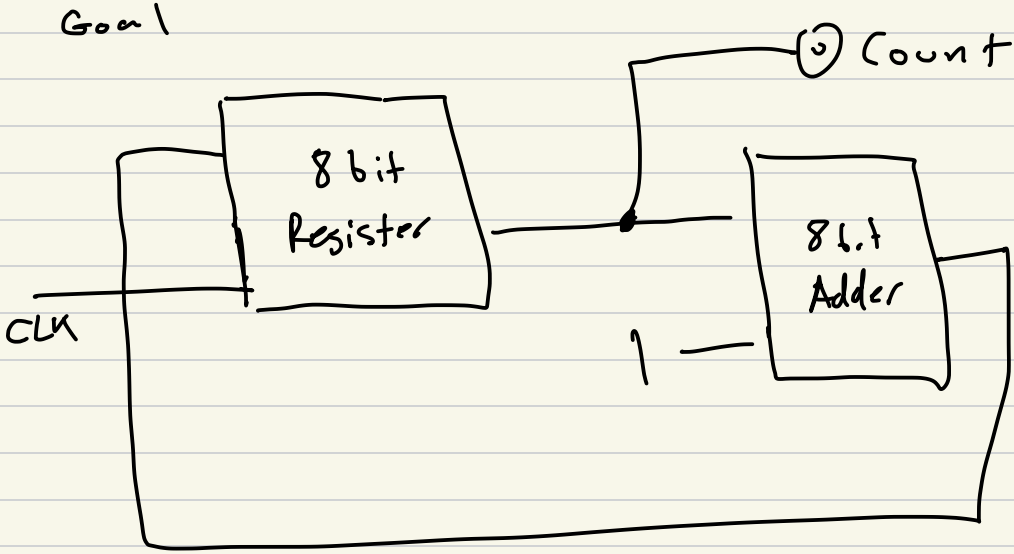
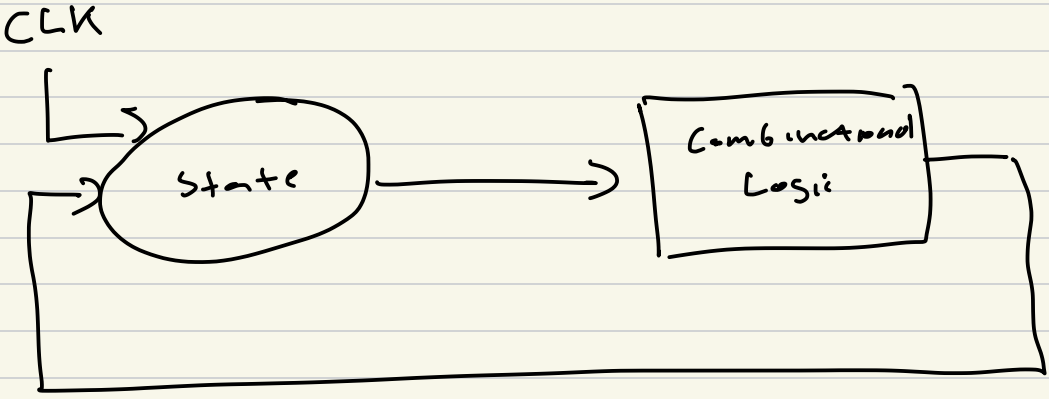
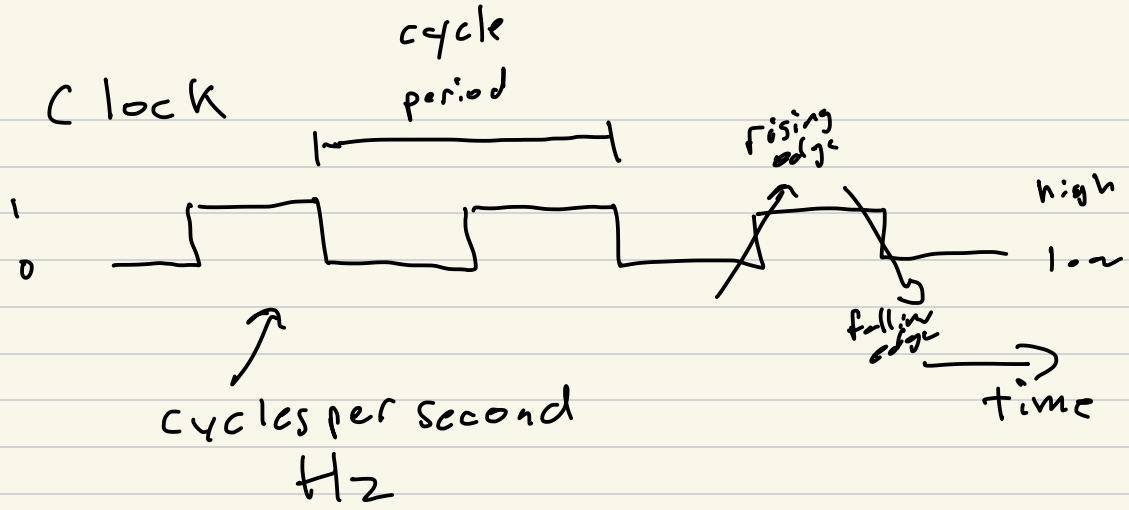
CS 315-01 Lab Sequential Logic

Goal

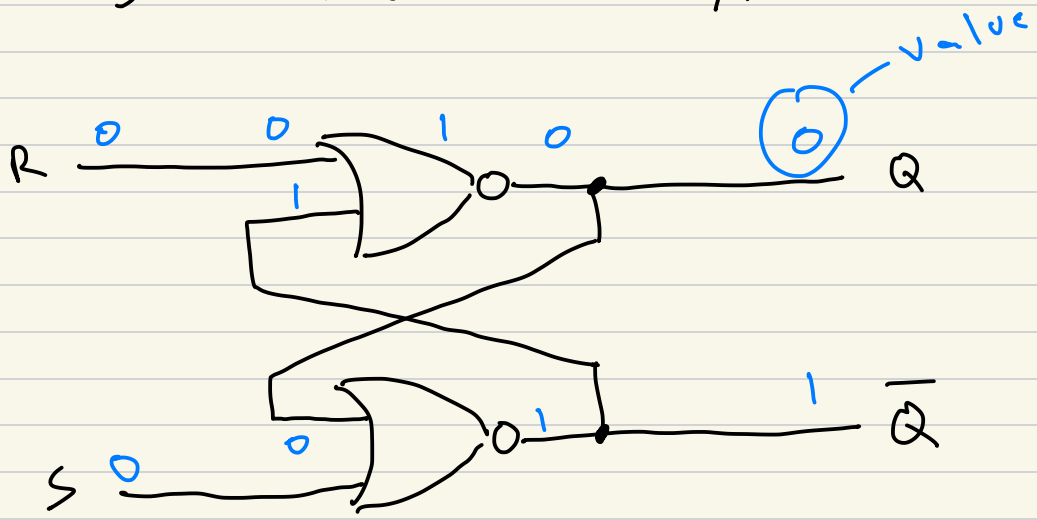


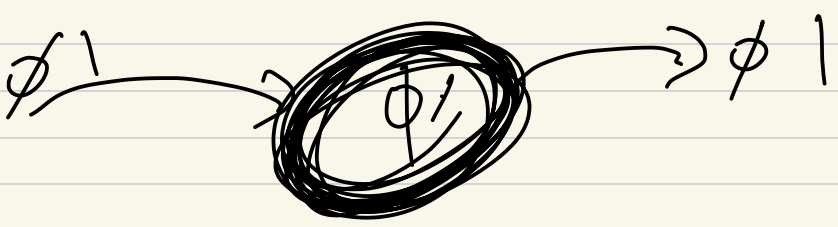


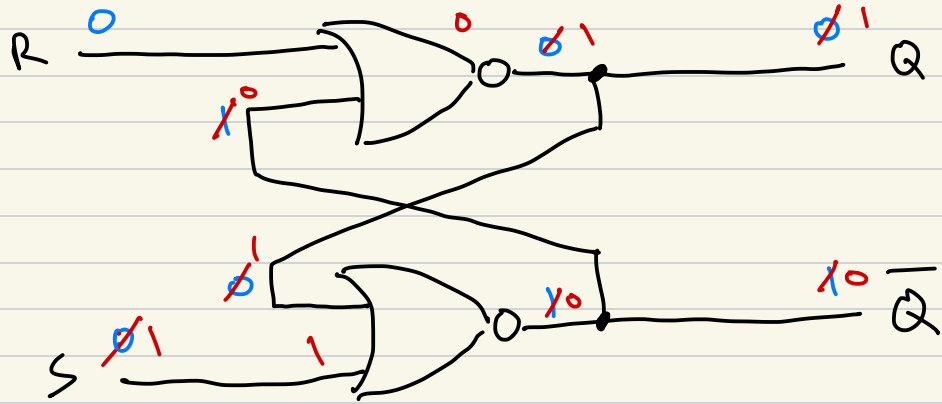


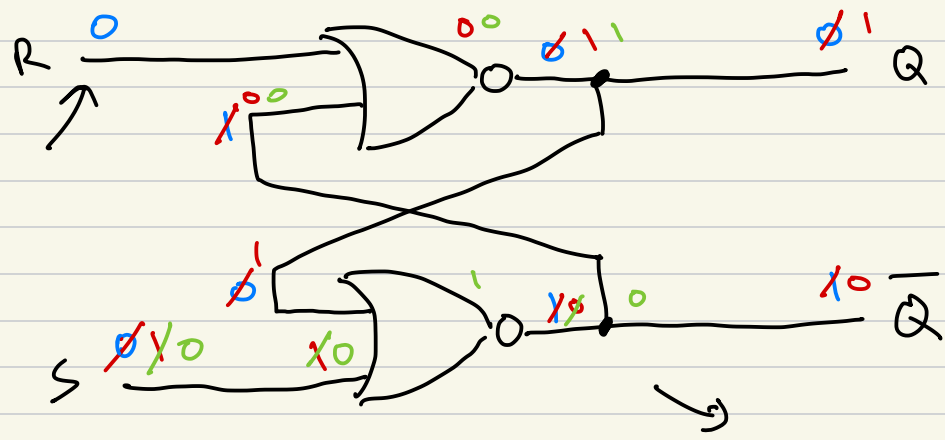
How to store a 1 bit value?

SR Latch Set/Reset





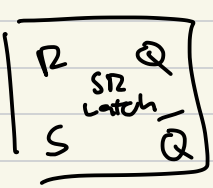




R	S	Q	$\overline{Q}$
0	0	0	1
0	1	1	0
0	0	1	0
1	0	0	1
0	0	0	1
1	1	X	X

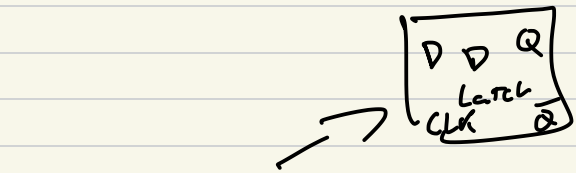
time ↓

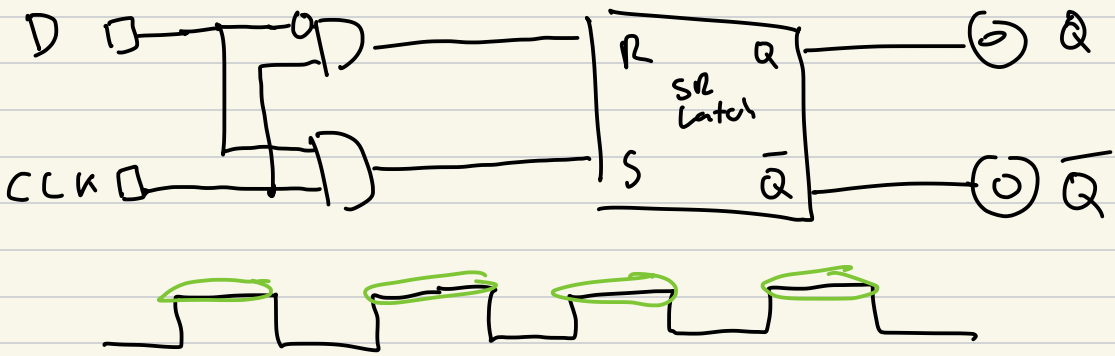
undefined



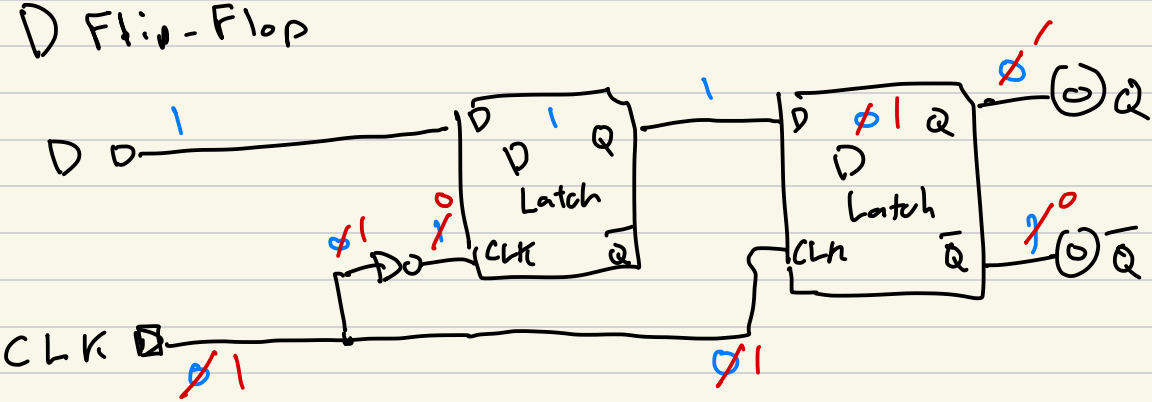
SR Latch → D Flip-flop → 1 bit Resister
→ N bit Resister → Counter

D Latch



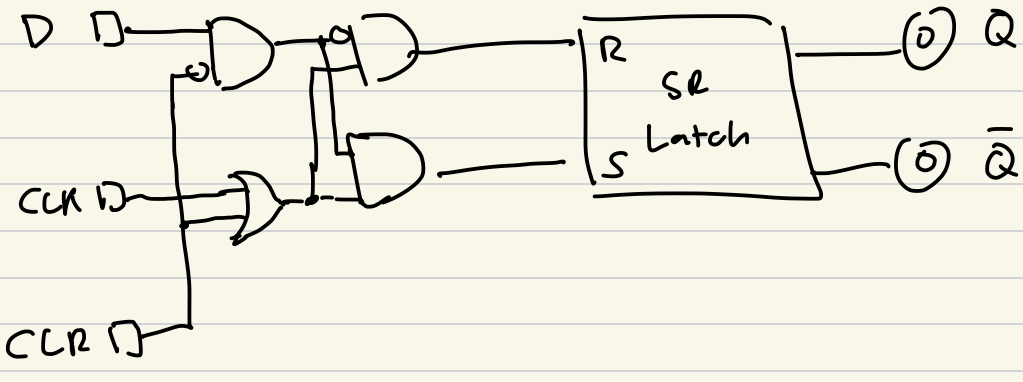


D Flip-Flop



1 bit resister

D Latch with CLR



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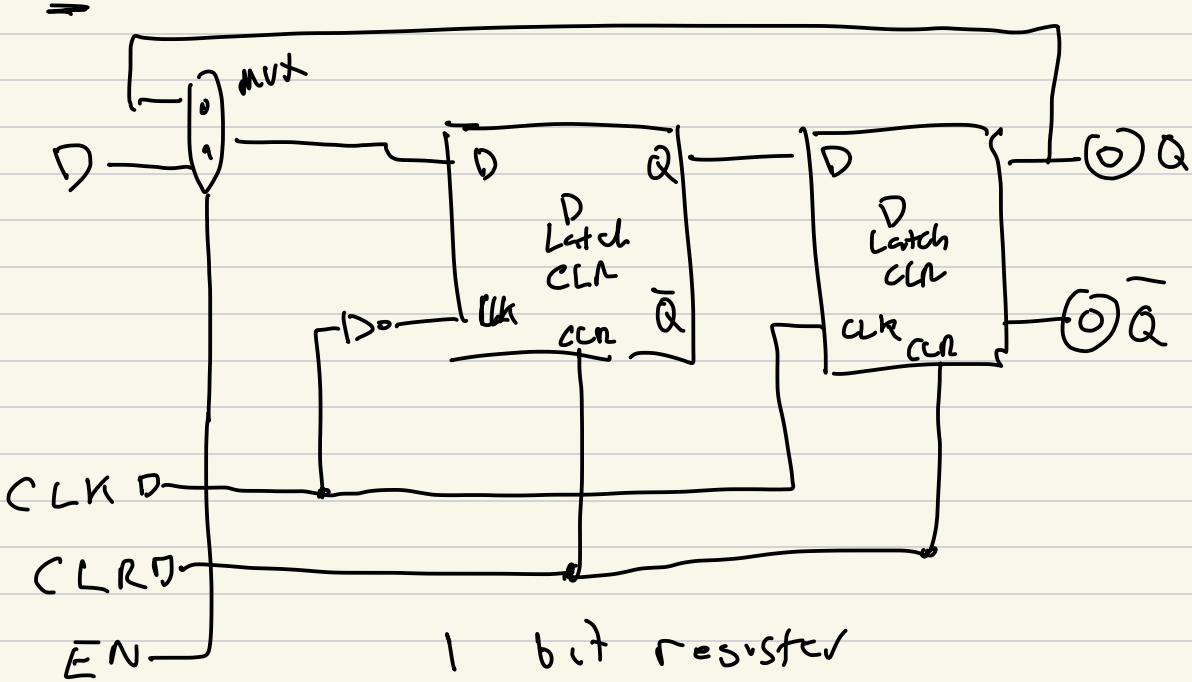

1 bit resister

4 bit register